REMARKS

Claims 1-30 and 32-33 are pending in this application. Claims 1-19 are withdrawn from consideration. By this Amendment, the title and claims 20-22, 26 and 29 are amended and claim 31 is cancelled. Attached hereto is a marked up version of the changes to the claims by the current amendment. The attached page is titled "Version With The Markings to Show Changes Made." Various amendments have been made to the claims for clarity, and for reasons unrelated to patentability. Unless specifically addressed below, each of the claim amendments is to provide further clarity and/or to refocus on specifically claimed features.

The Office Action objects to the drawings because the claimed third and fourth metal layers (claim 31) are not shown in the drawings. By this amendment, claim 31 is cancelled. Thus, the objection to the drawings is moot.

The Office Action objects to the disclosure because of an informality. In particular, the Office Action recommends amending "high" on page 17, line 13 to --higher--. However, this change has already been made in the May 7, 2001 Substitute Specification. See paragraph 32 of the Substitute Specification. Withdrawal of the objection to the disclosure is respectfully requested.

The Office Action indicates that the title is not descriptive. It is respectfully submitted that the new title is indicative of the invention to which the claims are directed.

The Office Action also objects to claims 20-33 because of informalities and rejects claims 20-33 under 35 U.S.C. § 112, second paragraph. It is respectfully submitted that the above amendments to the claims obviate the grounds for objection and rejection. In particular, claim 20 is amended to change "boring" to

--etching--, and to change "electrode" to --electrodes--. Claim 26 is also amended to change "continuously" to --continuous--. Claim 20 is also amended to change "for burying the inside" to --for providing on an inside--. Claim 21 has been amended to make it clear which layers are being referenced. Still further, claim 29 is amended to refer to "a continuous second electrode" and "to provide within the spaces". Claim 31 has also been cancelled. Withdrawal of the objection and rejection is respectfully requested.

The Office Action also rejects claims 20-26, 30, 32 and 33 under 35 U.S.C. § 103(a) by U.S. Patent 5,837,578 to Fan et al. (hereafter Fan) in view of U.S. Patent 5,854,104 to Onishi et al. (hereafter Onishi). The rejections are respectfully traversed.

The Office Action admits that Fan does not teach many of the features of the claims, such as forming a metal or metal compound for forming the lower electrode, patterning first and second conductive layers to form second electrodes, depositing a third inter-layer insulating film to cover the second electrodes, and forming connection holes reaching the second electrodes and the first layer wiring.

The Office Action relies on Onishi as teaching using a metal to form the lower electrode of a ferroelectric capacitor, patterning first and second conductive layers to form second electrodes and forming a third insulating film and forming a connection hole to the second electrode. See Onishi's column 7, lines 38-43.

Independent claim 20 recites depositing a third inter-layer insulating film covering the second electrodes, and forming a first connection hole reaching the second electrode and a second connection hole reaching the first layer wiring, by etching. Independent claim 20 also recites that the second conductive layer

comprises a tungsten film and the third inter-layer insulating film comprises a silicon oxide film.

It is respectfully submitted that Onishi does not teach or suggest at least these features of independent claim 20. As discussed in the present application, the upper layer of the upper electrode of the capacitor may function as an etching stopper during the etching step for forming openings 56 and 57. See paragraphs 92-94 of the Substitute Specification, for example. Onishi does not teach or suggest etching a second connection hole in a third inter-layer insulating film that extends over a first wiring and an etching stopper during the etching step. More specifically, Onishi does not teach or suggest forming the first connection hole reaching the second electrode and the second connection hole reaching the first layer wiring by etching as recited in independent claim 20. Onishi also does not teach or suggest that the second conductive layer comprises a tungsten film and the third insulating film comprises silicon oxide film. Thus, Fan and Onishi do not suggest all the features of claim 20. Independent claim 20 therefore defines patentable subject matter. Claim 21 depends from claim 20 and therefore also defines patentable subject matter.

Independent claim 22 recites that the formation step of the second electrode includes the steps of: forming a first metal layer by a chemical vapor phase growing method containing oxygen over the capacitance insulating film, and forming a second metal layer not containing oxygen over the first metal layer. The first conductive layer directly contacts to the second metal layer. As discussed in the present application, in order to prevent forming an oxide film between an upper electrode and a plug electrode connecting the upper electrode, the upper electrode may include a first metal film containing oxygen and a second metal film not containing oxygen. See paragraph 85 of the Substitute Specification, for example.

Onishi does not teach or suggest how to form the Pt film 15 and the TiN film 16. As such, Onishi does not suggest a method wherein the formation of the second electrode includes forming a second metal layer not containing oxygen over the first metal layer in combination with the first conductive directly contacts to the second metal layer. Accordingly, Fan and Onishi do not suggest all the features of claim 22. Independent claim 22 therefore defines patentable subject matter. Claims 23-25 depend from claim 22 and therefore also define patentable subject matter.

Independent claim 26 recites forming a first metal layer over the capacitance insulating film and forming a second metal layer having a greater film thickness than the first metal layer over the first metal layer. The second metal layer has a lower resistivity than the first metal layer. As discussed in the present application, the upper electrode may include two layers of metal film (i.e., a first metal film and a second metal film). The second metal film may be thicker than the first metal film because the resistivity of the second metal film is lower than the first metal film and the thin film has a lower stress than the thick film. See paragraphs 82-84 of the Substitute Specification, for example. Onishi discloses the thickness of the Pt film 15 and the TiN film 16. However, Onishi does not teach or suggest the resistivity of the Pt film 15 or the TiN film 16. As such, Fan and Onishi do not teach or suggest all the features of independent claim 26. Independent claim 26 therefore defines patentable subject matter. Claims 27-28 depend from claim 26 and therefore also define patentable subject matter.

Independent claim 29 recites forming a first metal layer over the capacitance insulating film in such a fashion as to provide within the space between the mutually spaced-apart first electrodes, and forming the second metal layer over the first metal layer. As discussed in the present application, the second metal film may be formed

by a sputtering method because the first metal film buries (or is provided within) the space between the first electrodes. See paragraph 78-82 of the Substitute Specification, for example. Onishi only shows one capacitor. Therefore, Onishi does not suggest that the first metal film is provided within the spaces between the first electrodes. As such, Fan and Onishi do not suggest all the features of independent claim 29. Independent claim 29 therefore defines patentable subject matter. Claims 30, 32 and 33 depend from claim 29 and therefore also define patentable subject matter.

In view of the foregoing, it is respectfully submitted that each of claims 20-30 and 32-33 define patentable subject matter. Withdrawal of the outstanding rejections are respectfully requested.

CONCLUSION

In view of the foregoing, it is respectfully submitted that the above- identified application is in condition for allowance. Favorable consideration and prompt allowance of claims 20-30 and 32-33 are respectfully requested.

It is respectfully requested that any shortage in the fee be charged to the account of Antonelli, Terry, Stout & Kraus, LLP, Account No. 01-2135 (Case No. 501.39149X00).

Respectfully submitted,

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Versi n With The Markings to Show Changes Mad

IN THE CLAIMS

Claims 20, 21, 22, 26 and 29 have been amended as follows:

20. (Amended) A method of producing a semiconductor integrated circuit device comprising the steps of:

(a) forming bit lines and a first layer wiring over MISFET on a main plane of a semiconductor substrate through a first inter-layer insulating film, forming a second inter-layer insulating film and an electrode-forming insulating film, and [boring] etching holes in said electrode-forming insulating film; Fig 3

(b) forming a metal or a metal compound for [burying the] providing on an inside of said holes, and then forming [columnar or] cylindrical first electrodes [by removing said electrode-forming insulating film or] by forming a metal film or a metal compound film covering the inner wall of said holes; Fig 4-6

(c) depositing a [ferroelectric or high] dielectric capacitance insulating film to cover said first [electrode] electrodes, and depositing further a first conductor layer and a second conductor layer; Fig. 7-9

(d) patterning said first and second conductor layers to form second electrodes; and Fig 10

(e) depositing a third inter-layer insulating film covering said second electrodes, and forming a first connection [holes] hole reaching said second electrode and a second connection [holes] hole reaching said first layer wiring, by etching, wherein said second conductor layer comprises a tungsten film and said third inter-layer insulating film comprises a silicon oxide film. Fig 13-15

21. (Amended) A method of producing a semiconductor integrated circuit device according to claim 20, wherein, after said second conductive layer is etched

[in said etching step of said second electrode], said first conductive layer is etched by using said second conductive layer, that is patterned, as a mask.

22. (Amended) A method of producing a semiconductor integrated circuit device including the steps of:

(a) forming first electrodes on a first insulating film formed on a main plane of a semiconductor substrate;

(b) forming a capacitance insulating film over said first electrode;

(c) forming second electrodes over said capacitance insulating film;

(d) forming a second insulating film having an opening for exposing a part of said second electrode, on said second electrode; and

(e) forming a first conductor layer inside said opening; wherein:

the formation step of said second electrode includes the steps of:

(i) forming a first metal layer by a chemical vapor phase growing method containing oxygen over said capacitance insulating film; and

(ii) forming a second metal layer not containing oxygen over said first metal layer, wherein said first conductor layer directly contacts to said second metal layer.

26. (Amended) A method of producing a semiconductor integrated circuit device including the steps of:

(a) forming a plurality of mutually [spaced-part] spaced-apart first electrodes over a first insulating film formed on a main plane of a semiconductor substrate;

(b) forming a capacitance insulating film over said first electrodes; and

(c) forming [continuously] continuous second electrodes with respect to a plurality of said first electrodes, over said capacitance insulating film; wherein:

the formation step of said second electrodes includes the steps of:

(i) forming a first metal layer over said capacitance insulating film; and

(ii) forming a second metal layer having a greater film thickness than said first metal layer over said first metal layer, and said second metal layer has a lower resistivity than said first metal layer.

29. (Amended) A method of producing a semiconductor integrated circuit device including the steps of:

(a) forming a plurality of mutually spaced-apart first electrodes over a first insulating film formed on a main plane of a semiconductor substrate;

(b) forming a capacitance insulating film over said first electrodes; and

(c) forming [continuously] a continuous second [electrodes] electrode with respect to a plurality of said first electrodes, over said capacitance insulating film; wherein:

the formation step of said second [electrodes] electrode includes the steps of:

(i) forming a first metal layer over said capacitance insulating film in such a fashion as to [bury] provide within the spaces between said mutually spaced-apart first electrodes; and

(ii) forming said second metal layer over said first metal layer.